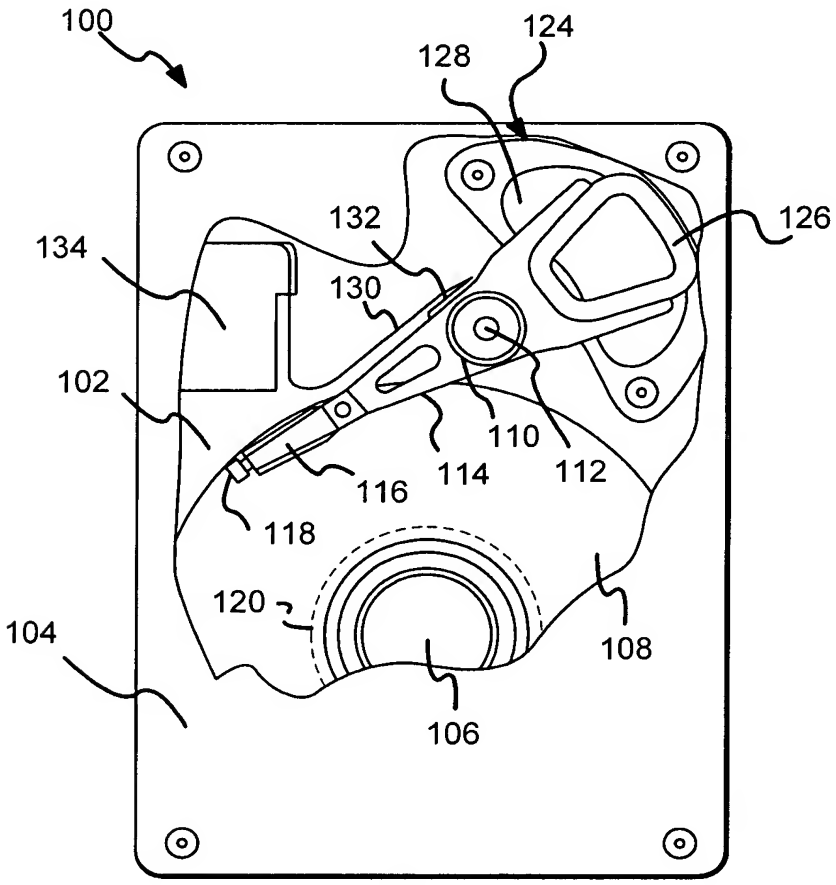

100
124
128
126
132
134
130
102
110
112
114
116
118
120
104
108
106

FIG.1

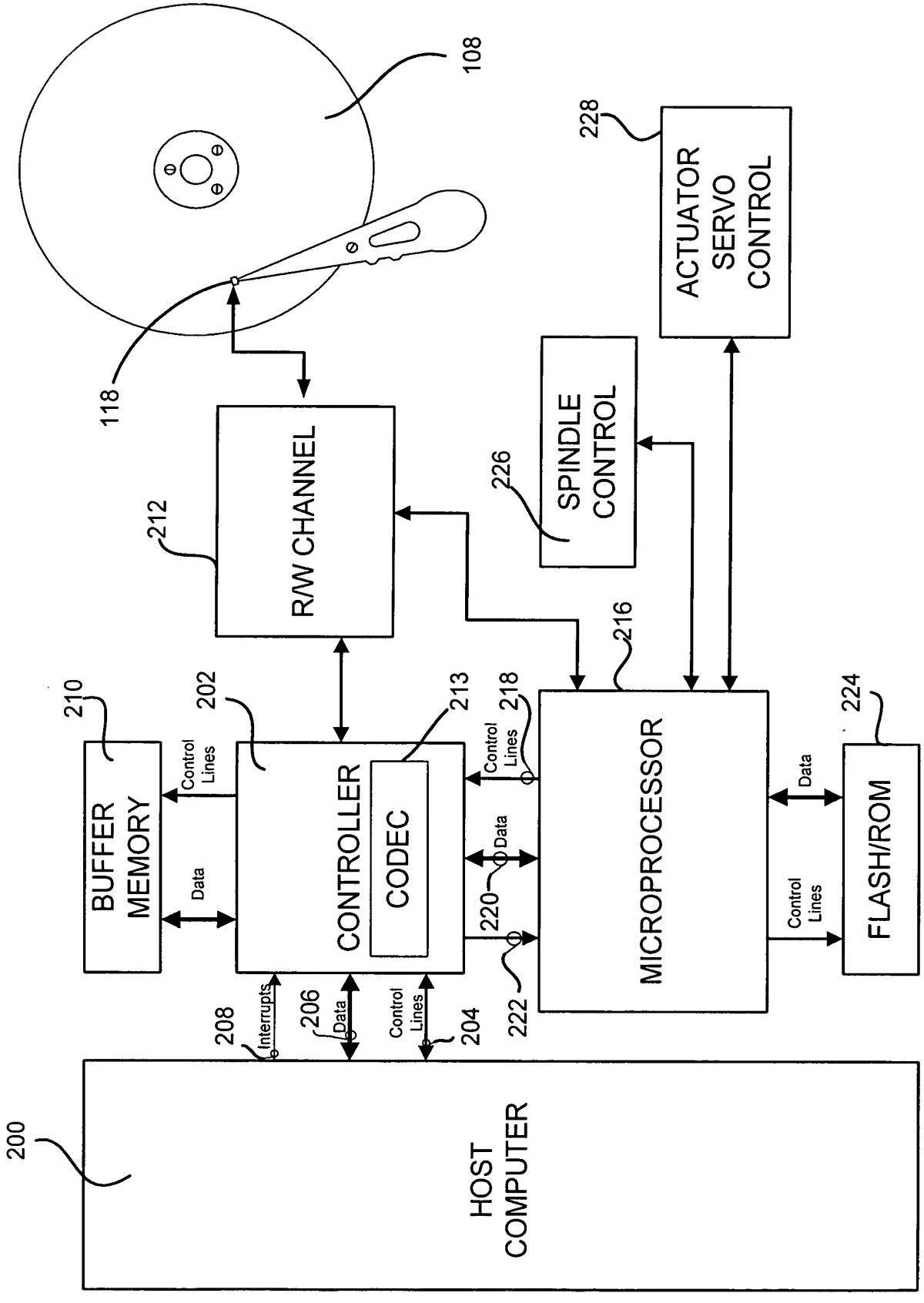

108
118
228
ACTUATOR SERVO CONTROL
212
R/W CHANNEL
226
SPINDLE CONTROL
216
210
202
213
218
224
BUFFER MEMORY
Control Lines
CONTROLLER
CODEC
Control Lines
MICROPROCESSOR
Data
FLASH/ROM
Data
Data
220
Control Lines
208
Interrupts
206
Data
Control Lines
204
222
200
HOST COMPUTER

FIG. 2

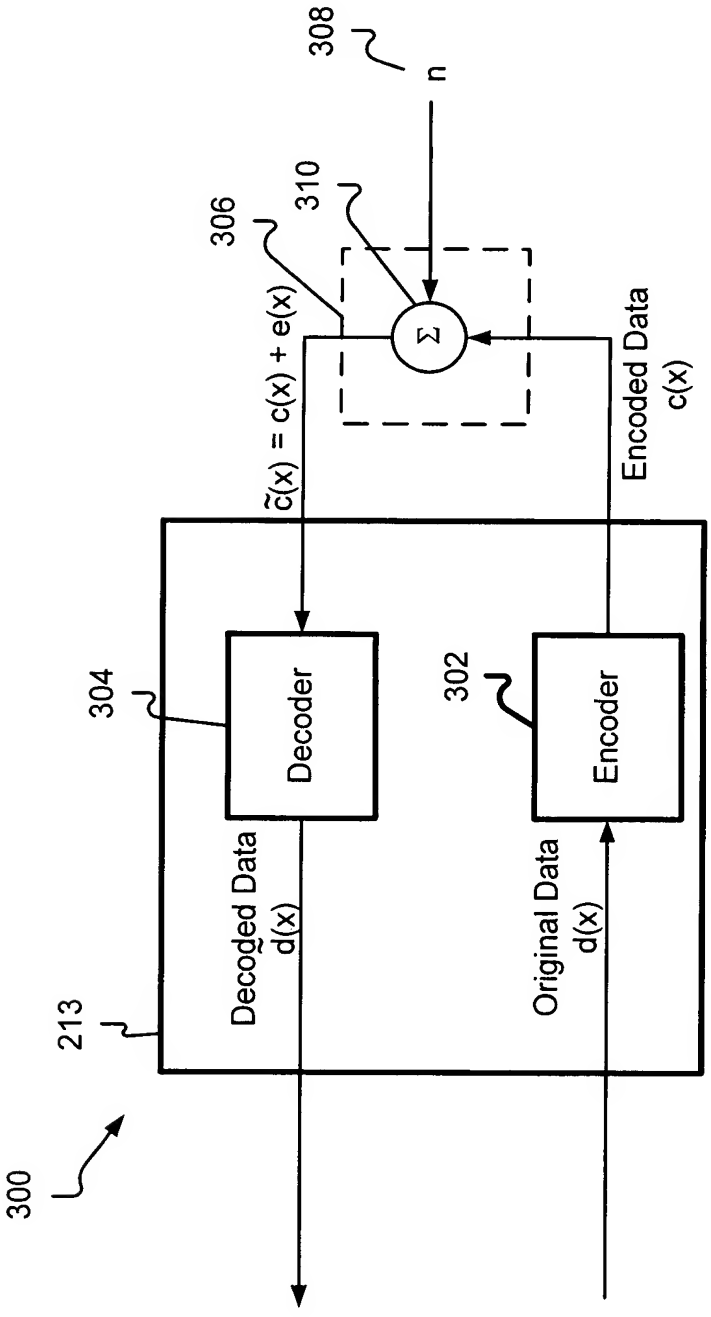

300
213
304
Decoder
Decoded Data
d(x)
302
Encoder
Original Data
d(x)
306
$\tilde{c}(x) = c(x) + e(x)$
310
Σ
308
n
Encoded Data
c(x)
Data Transfer System

FIG. 3

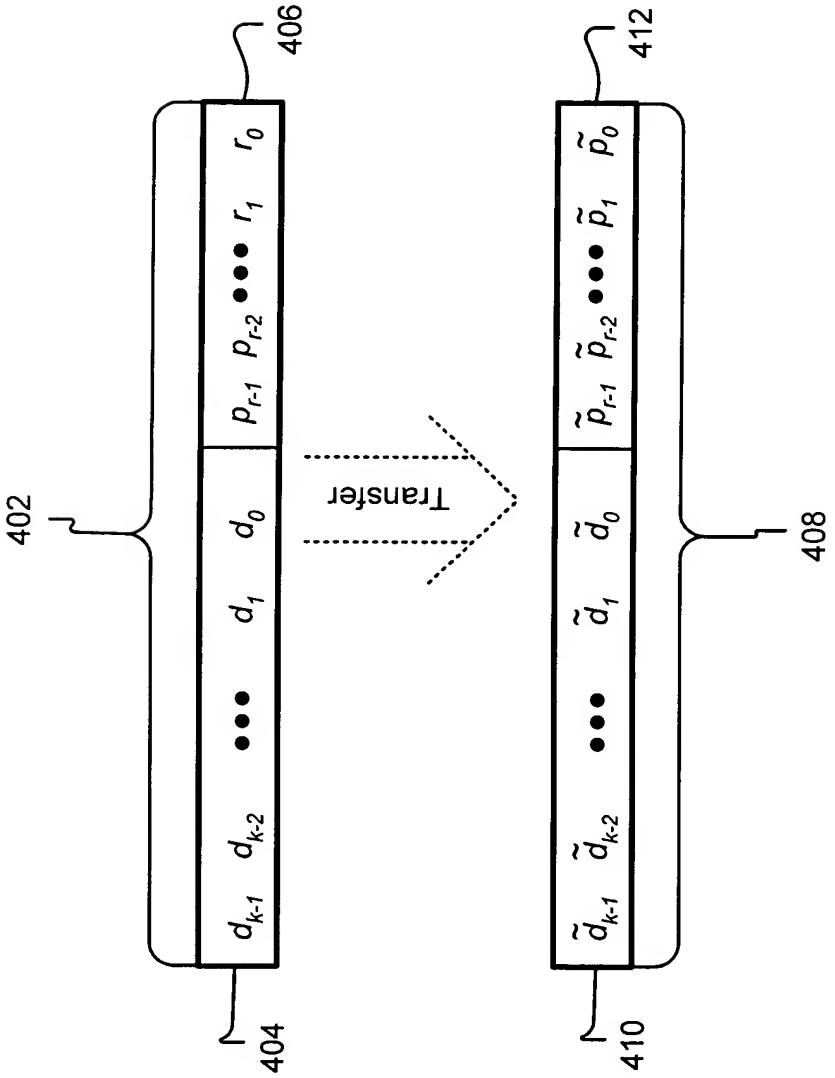

402
404
406
408
410
412
Transfer
d_0 d_1 d_{k-2} d_{k-1}
r_0 r_1 p_{r-2} p_{r-1}
$\tilde{d}_0$ $\tilde{d}_1$ $\tilde{d}_{k-2}$ $\tilde{d}_{k-1}$
$\tilde{p}_0$ $\tilde{p}_1$ $\tilde{p}_{r-2}$ $\tilde{p}_{r-1}$

FIG. 4

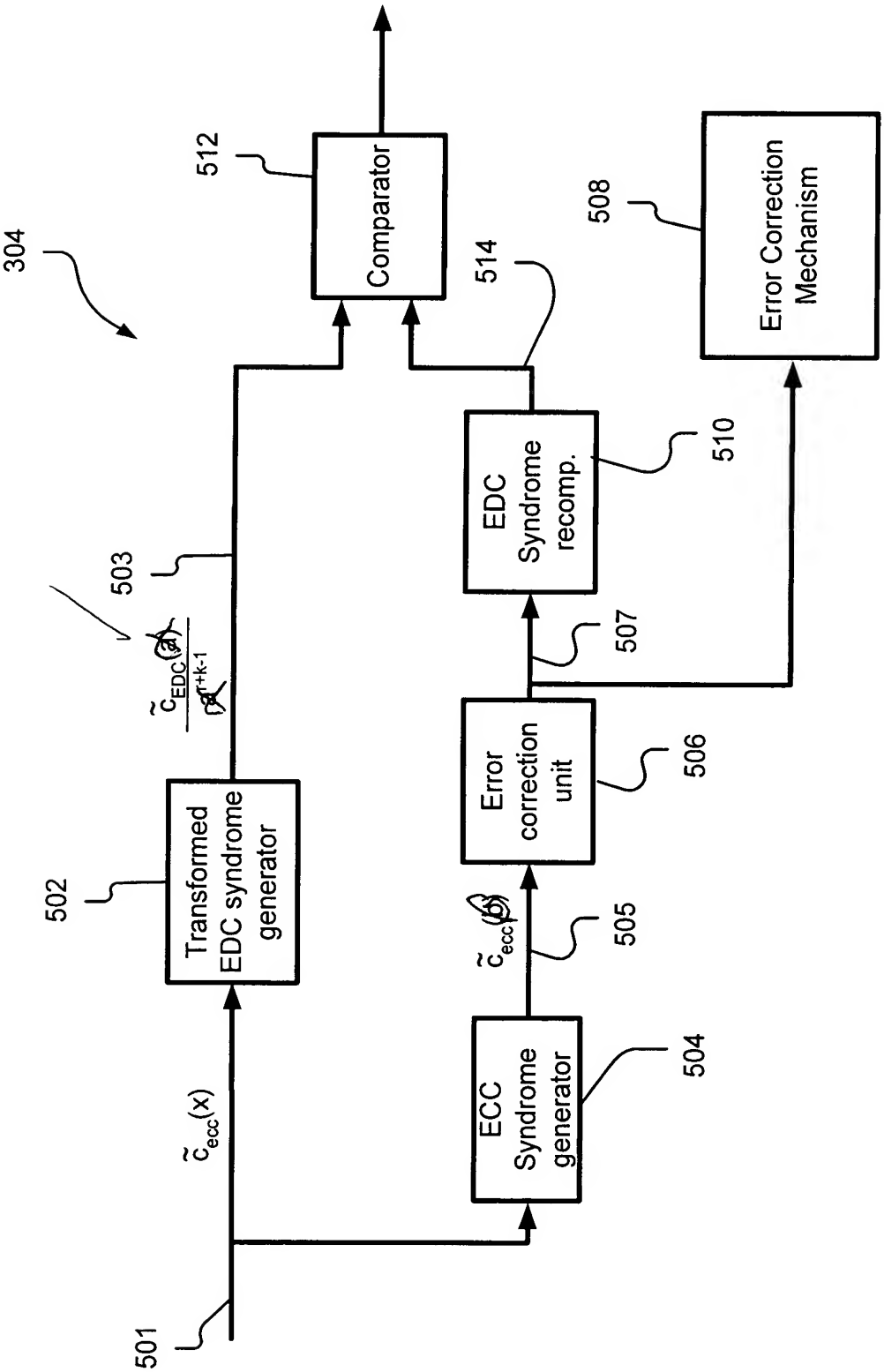

304
501
502
Transformed EDC syndrome generator
503
504
ECC Syndrome generator
505
Error correction unit
506
507
508
Error Correction Mechanism
510
EDC Syndrome recomp.
512
Comparator
514

FIG. 5

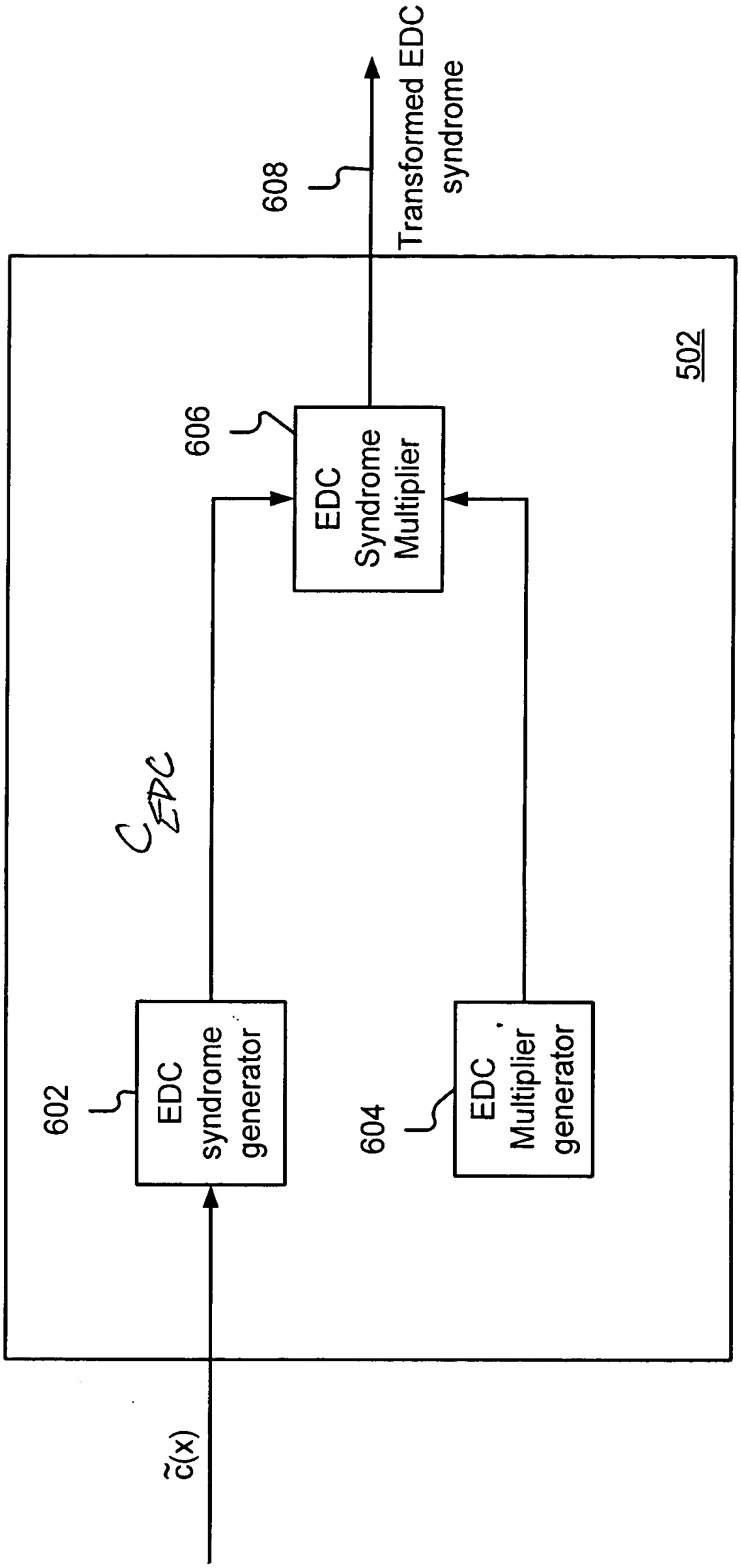

608
Transformed EDC syndrome
606
EDC Syndrome Multiplier
502
C_{EDC}
602
EDC syndrome generator
604
EDC Multiplier generator
$\tilde{c}(x)$
Transformed EDC syndrome generator

FIG. 6

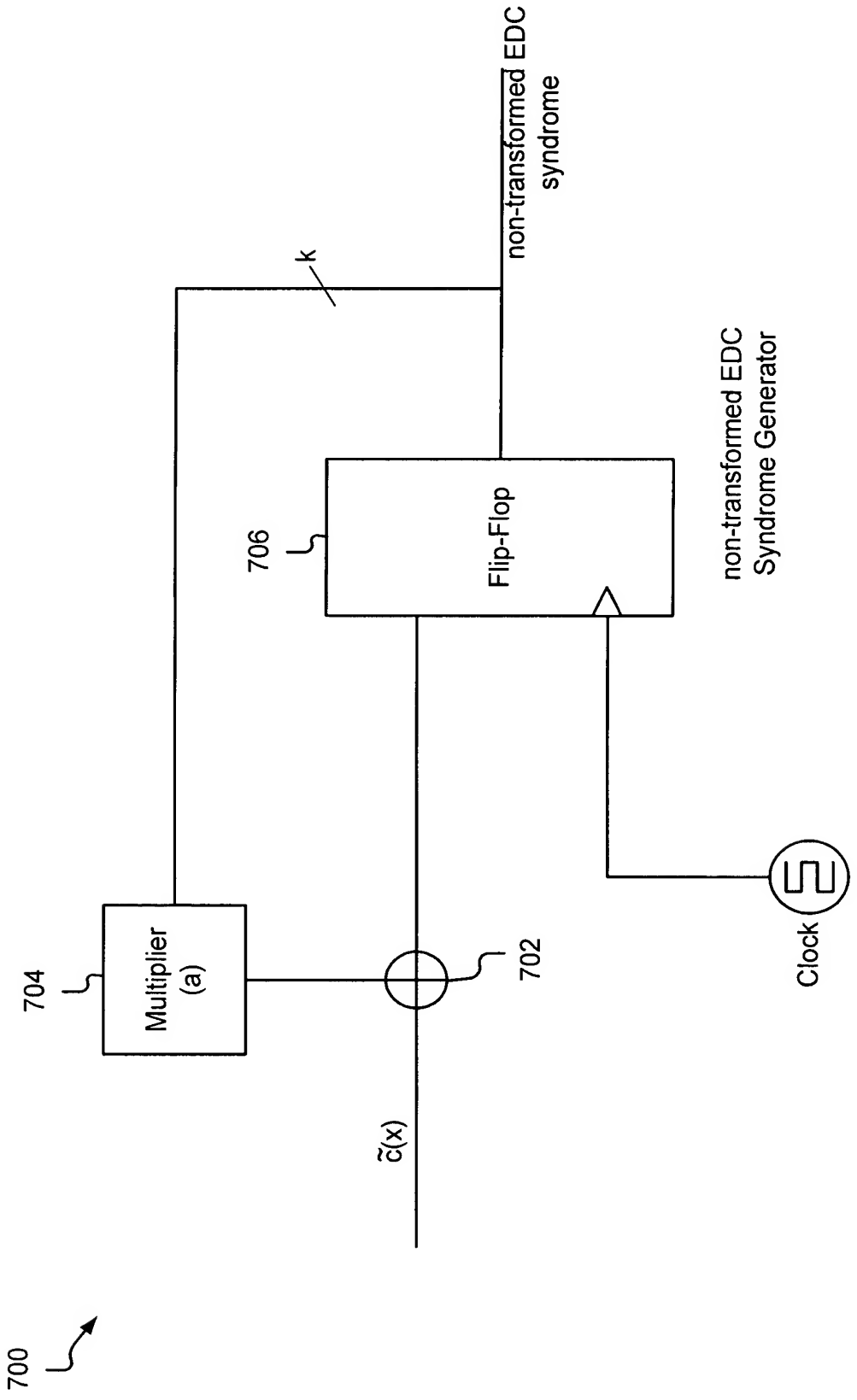

700
704
Multiplier
(a)
702
c̃(x)
706
Flip-Flop
k
non-transformed EDC
syndrome
non-transformed EDC
Syndrome Generator
Clock

FIG. 7

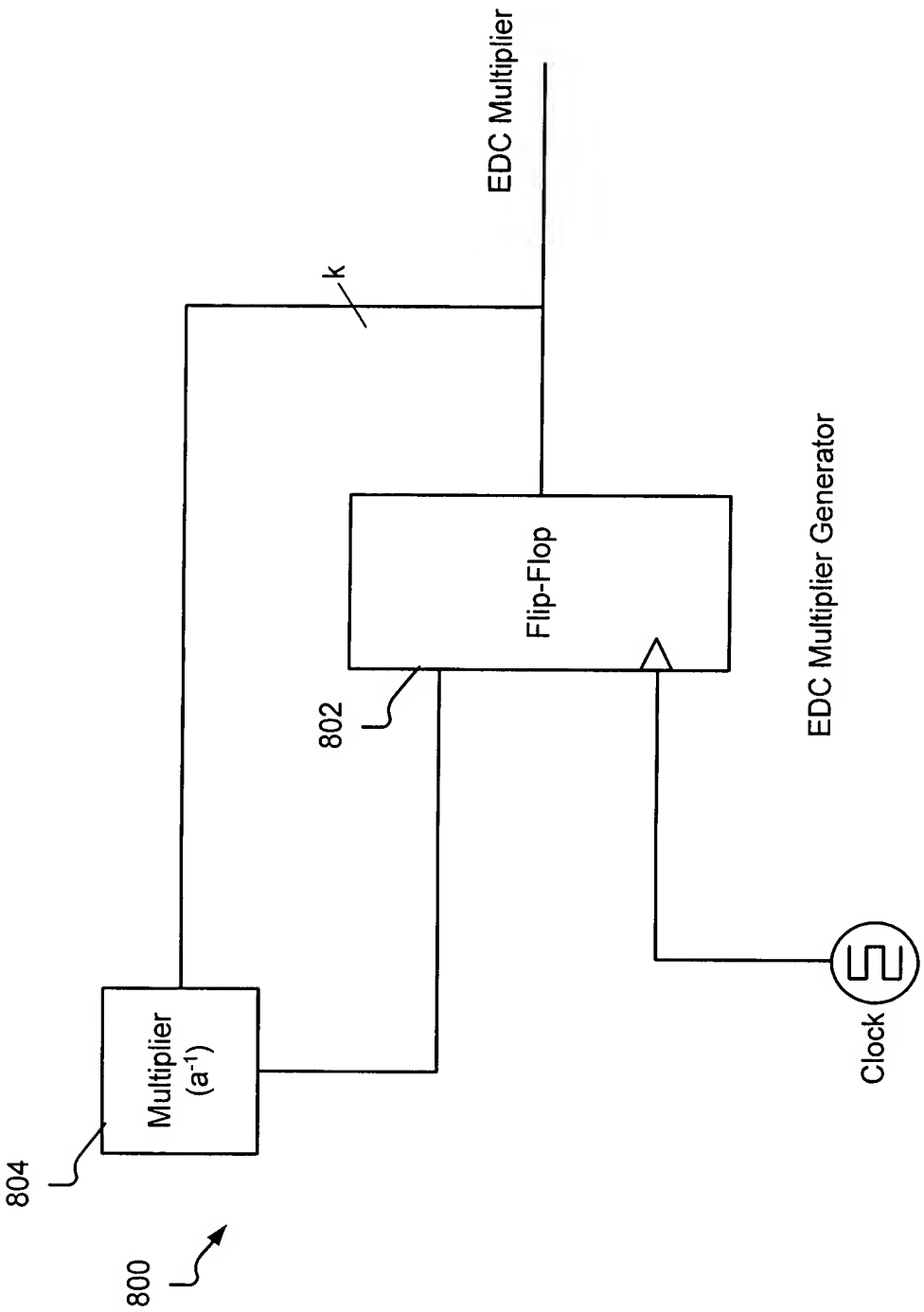

EDC Multiplier
k
Flip-Flop
802
EDC Multiplier Generator
Clock
Multiplier
(a-1)
804
800

FIG. 8

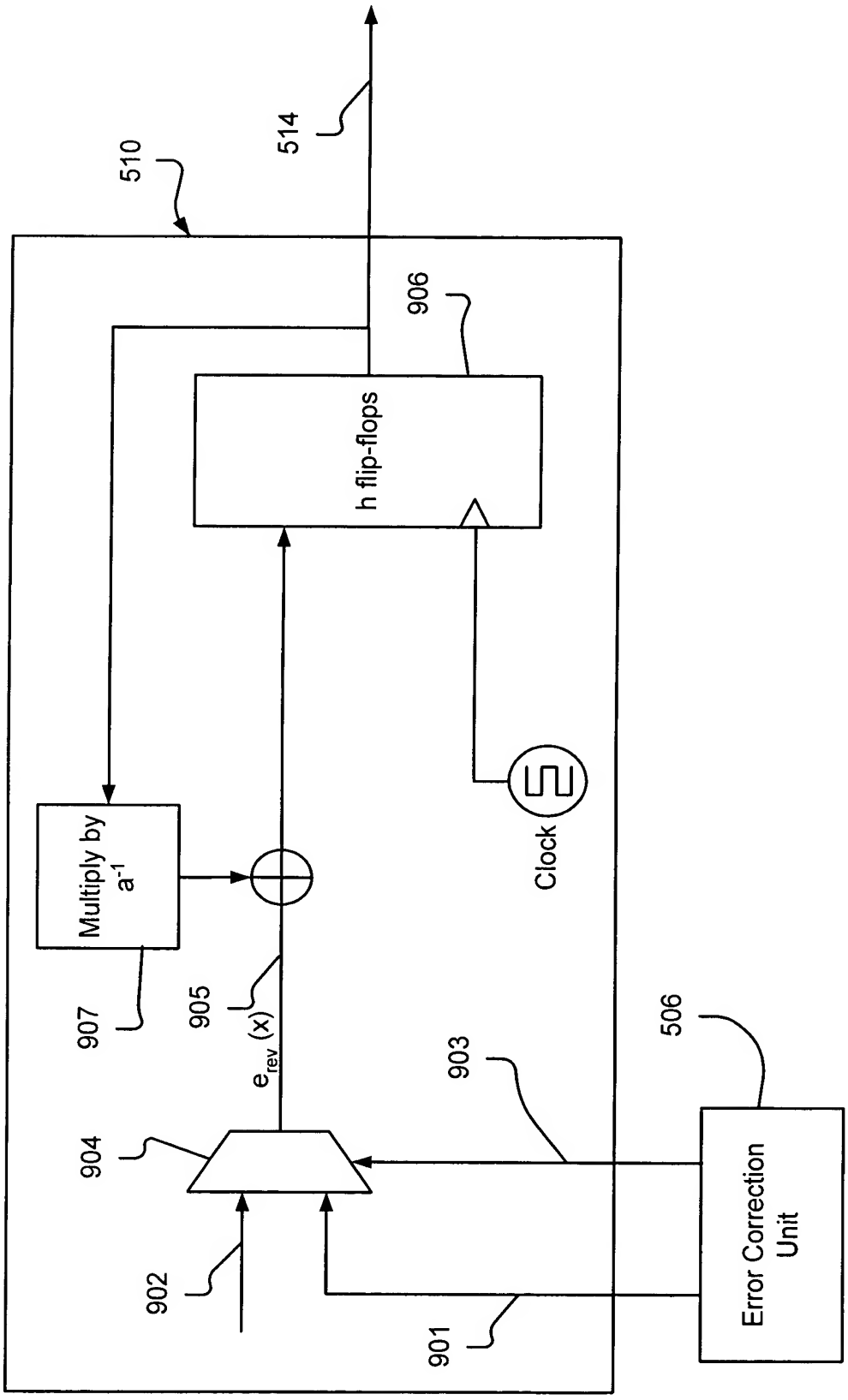

510
514
906
h flip-flops
Clock
Multiply by a^{-1}
907
905
$e_{rev}(x)$
903
506
904
902
901
Error Correction Unit

FIG. 9

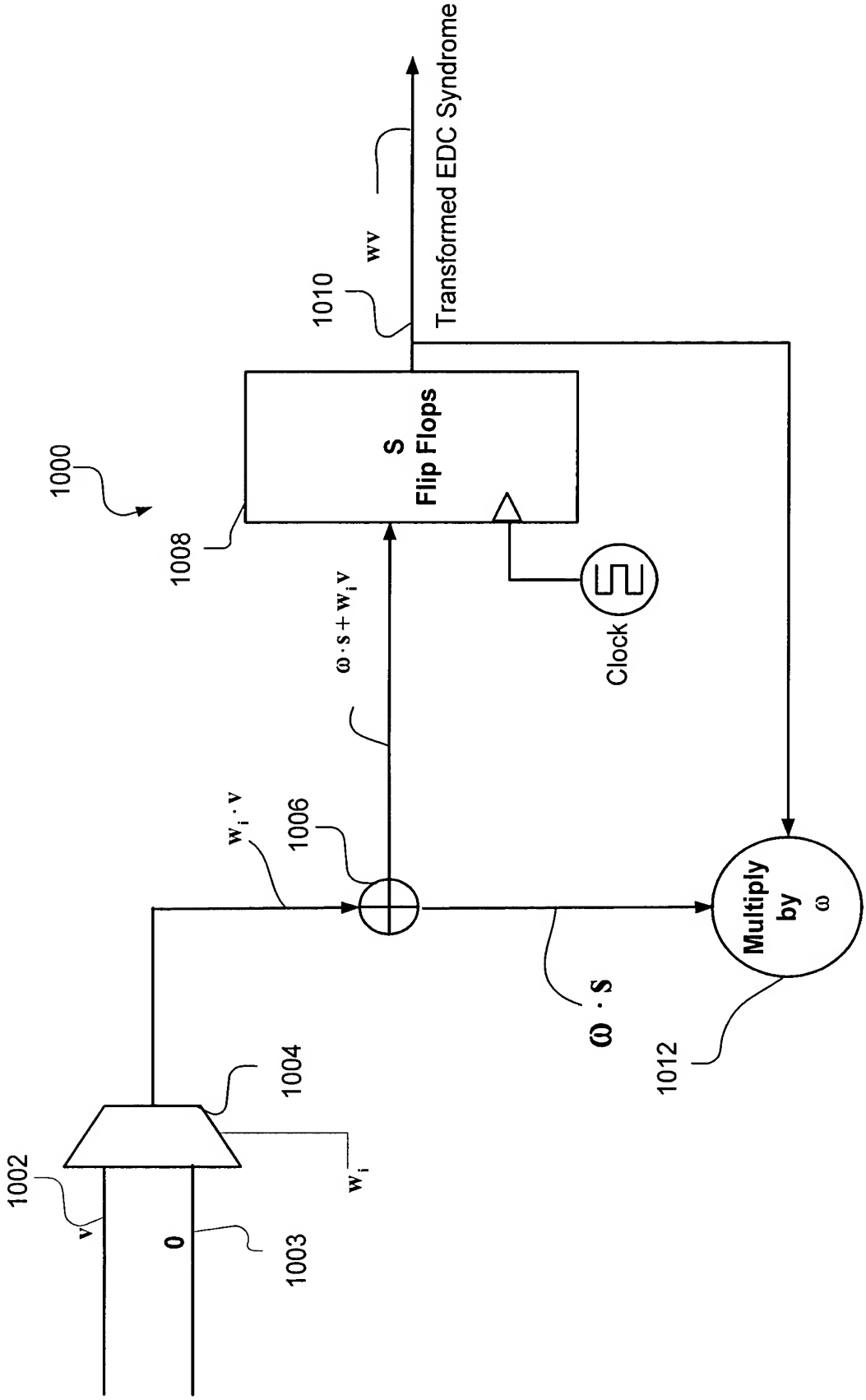

1000
1002
v
0
1003
1004
w_i
1006
$w_i \cdot v$
$\omega \cdot s + w_i v$
1008
S
Flip Flops
Clock
1010
wv
Transformed EDC Syndrome
$\omega \cdot s$
1012
Multiply by ω

FIG. 10

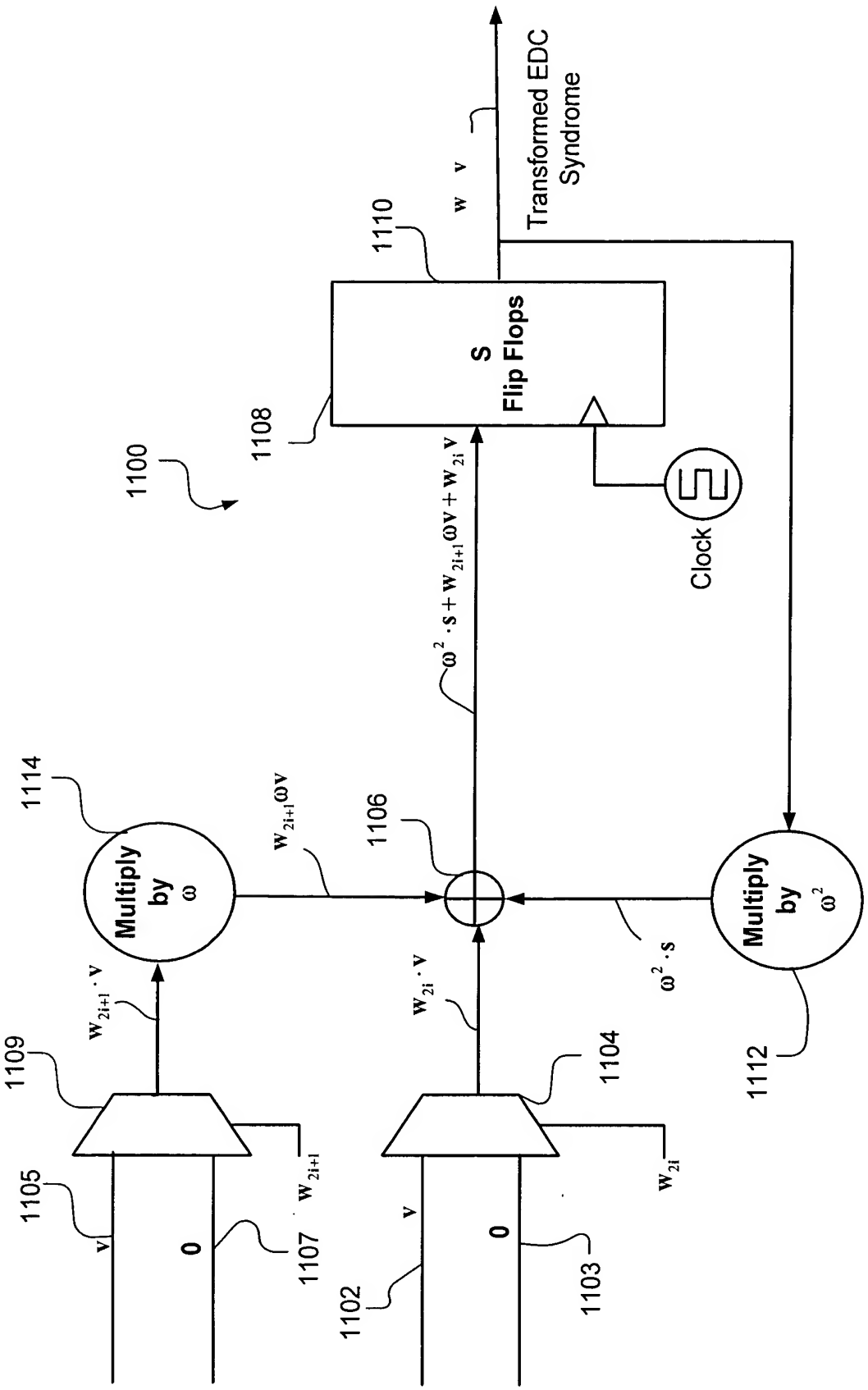

1100
1102
1103
1104
1105
1106
1107
1108
1109
1110
1112
1114
S
Flip Flops
Clock
Transformed EDC Syndrome
Multiply by ω
Multiply by ω²
0
0
v
v
w v
$\omega^2 \cdot s + w_{2i+1}\omega v + w_{2i} v$
$w_{2i+1}\omega v$
$w_{2i+1} \cdot v$
$w_{2i} \cdot v$
$\omega^2 \cdot s$
w_{2i+1}
w_{2i}

FIG. 11

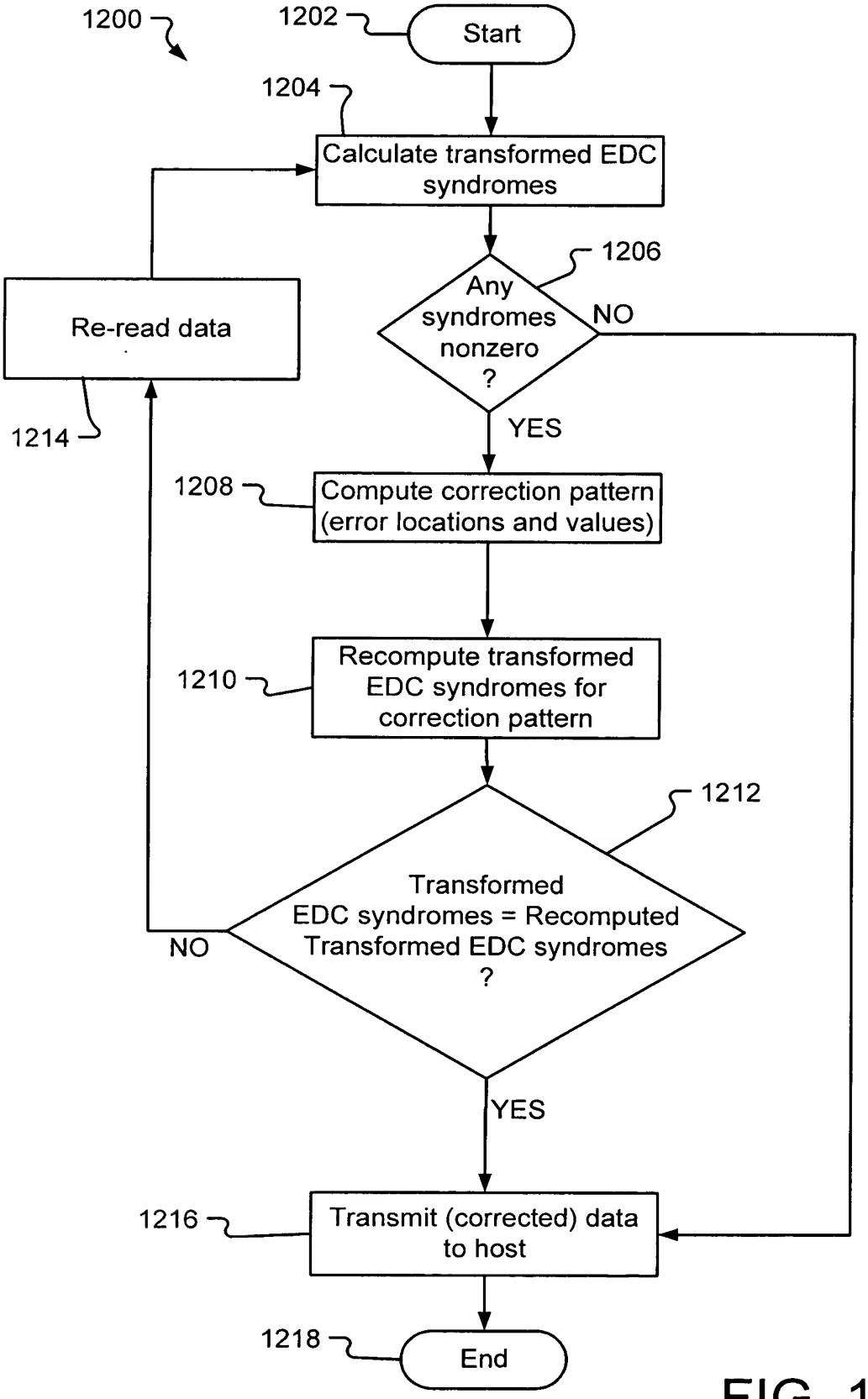
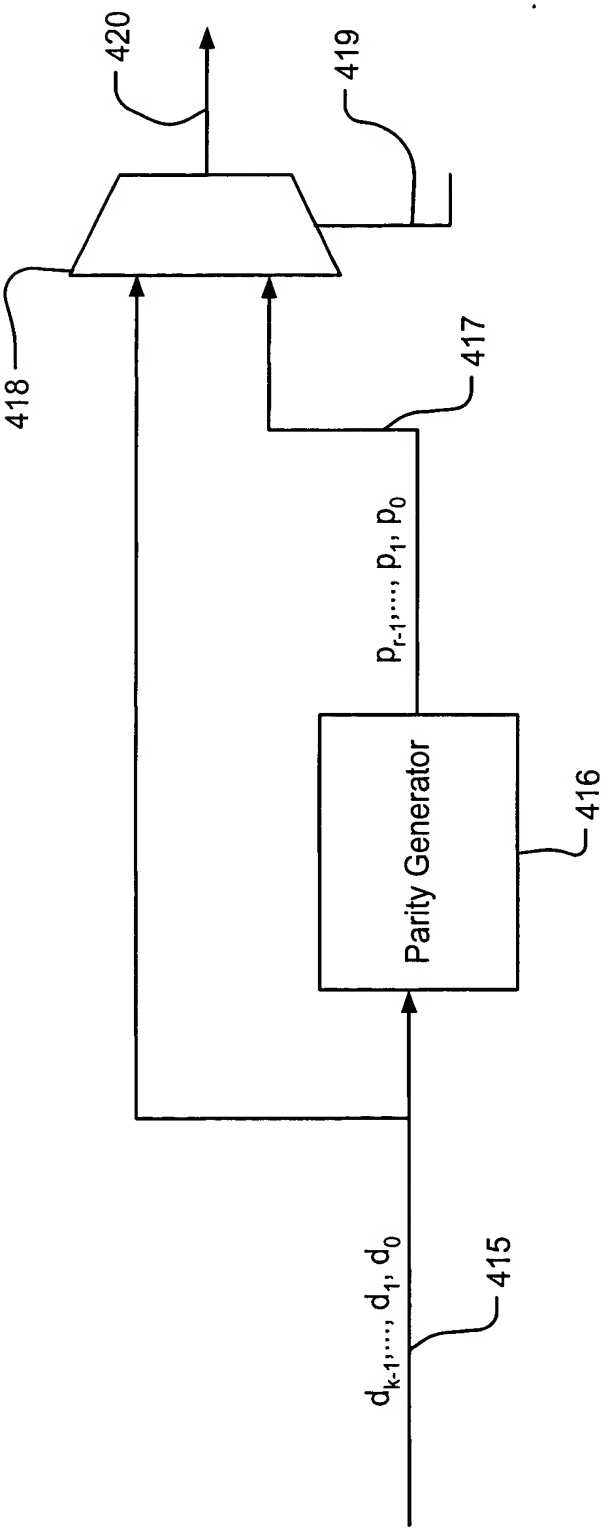
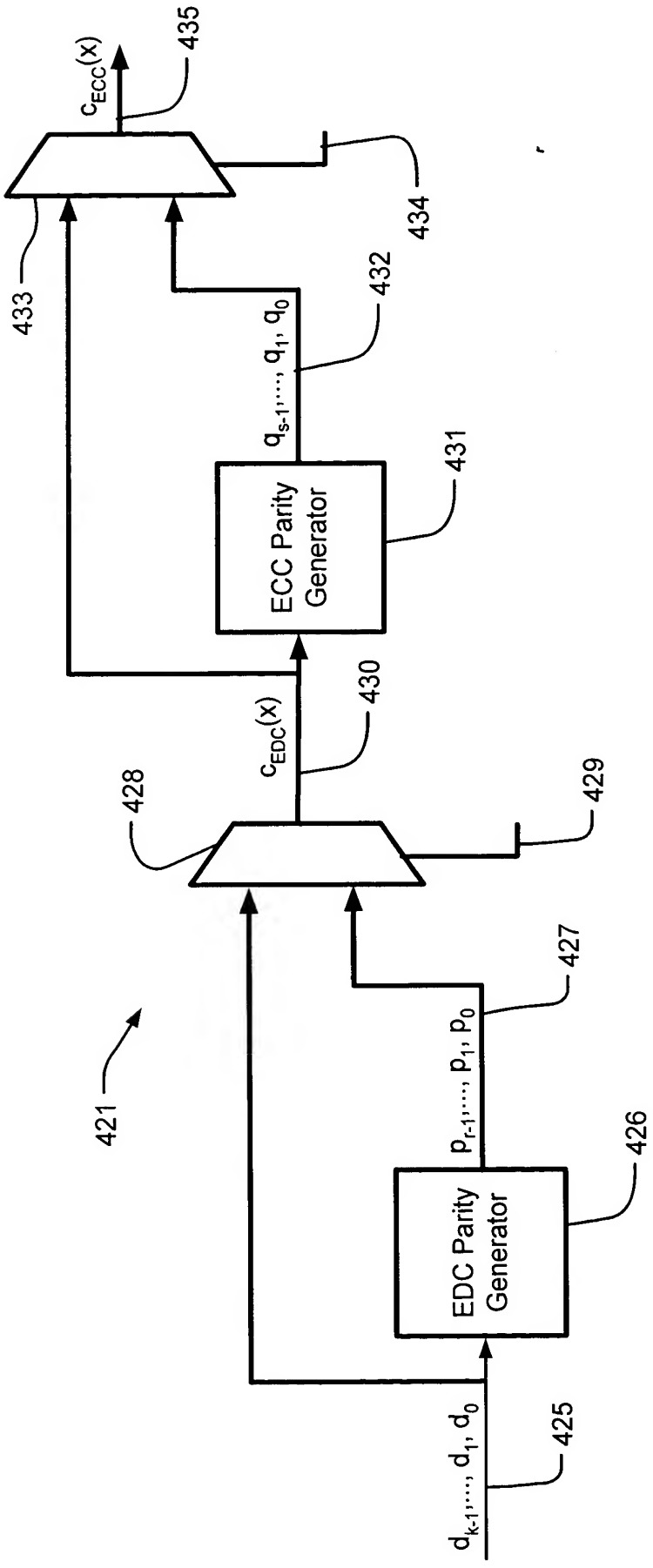

1200
1202
Start
1204
Calculate transformed EDC syndromes
1206
Any syndromes nonzero ?
NO
YES
Re-read data
1214
1208
Compute correction pattern (error locations and values)
1210
Recompute transformed EDC syndromes for correction pattern
1212
Transformed EDC syndromes = Recomputed Transformed EDC syndromes ?
NO
YES
1216
Transmit (corrected) data to host
1218
End

FIG. 12



Encoder for a Polynomial Code

FIG. 13



Encoder for a Concatenated System

FIG. 14

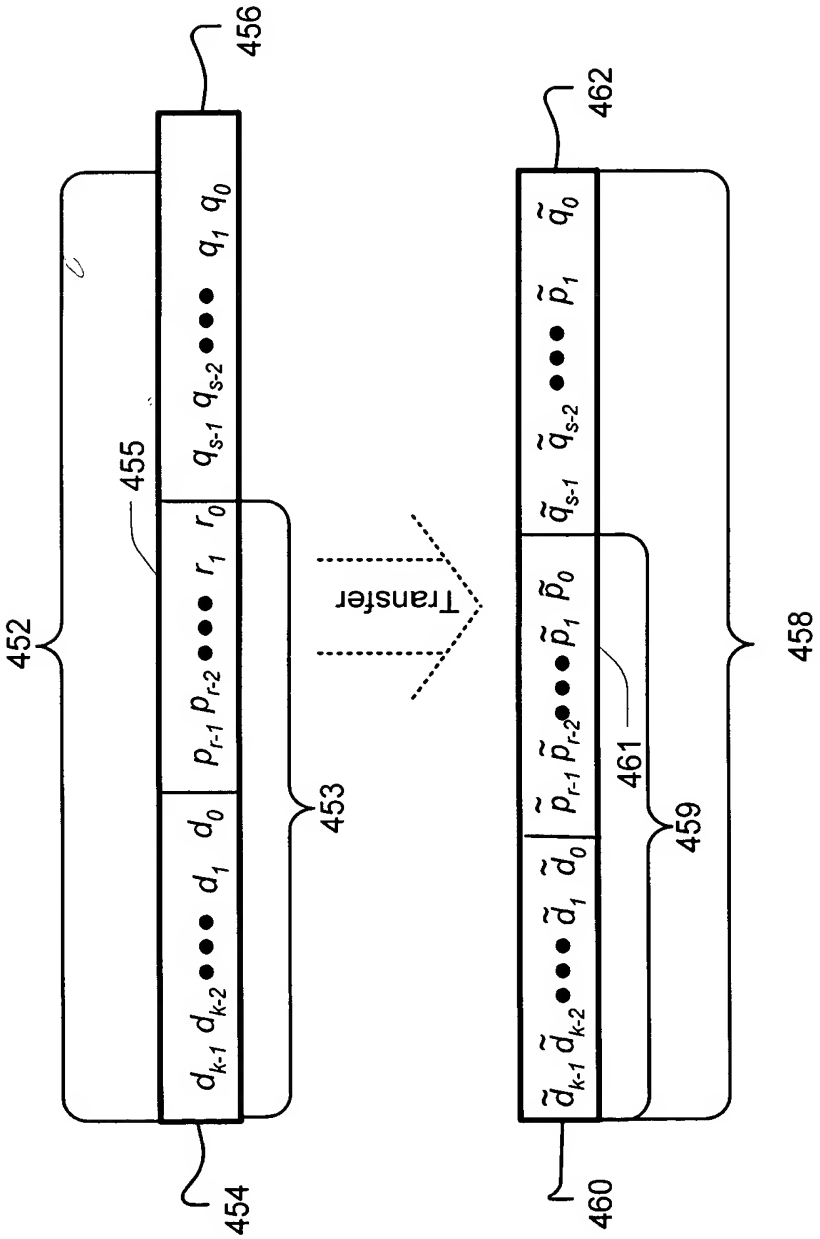

452
453
454
455
456
458
459
460
461
462
Transfer
d_{k-1} d_{k-2} ••• d_1 d_0
p_{r-1} p_{r-2} ••• r_1 r_0
q_{s-1} q_{s-2} ••• q_1 q_0
$\tilde{d}_{k-1}$ $\tilde{d}_{k-2}$ ••• $\tilde{d}_1$ $\tilde{d}_0$
$\tilde{p}_{r-1}$ $\tilde{p}_{r-2}$ ••• $\tilde{p}_1$ $\tilde{p}_0$
$\tilde{q}_{s-1}$ $\tilde{q}_{s-2}$ ••• $\tilde{p}_1$ $\tilde{q}_0$

FIG. 15

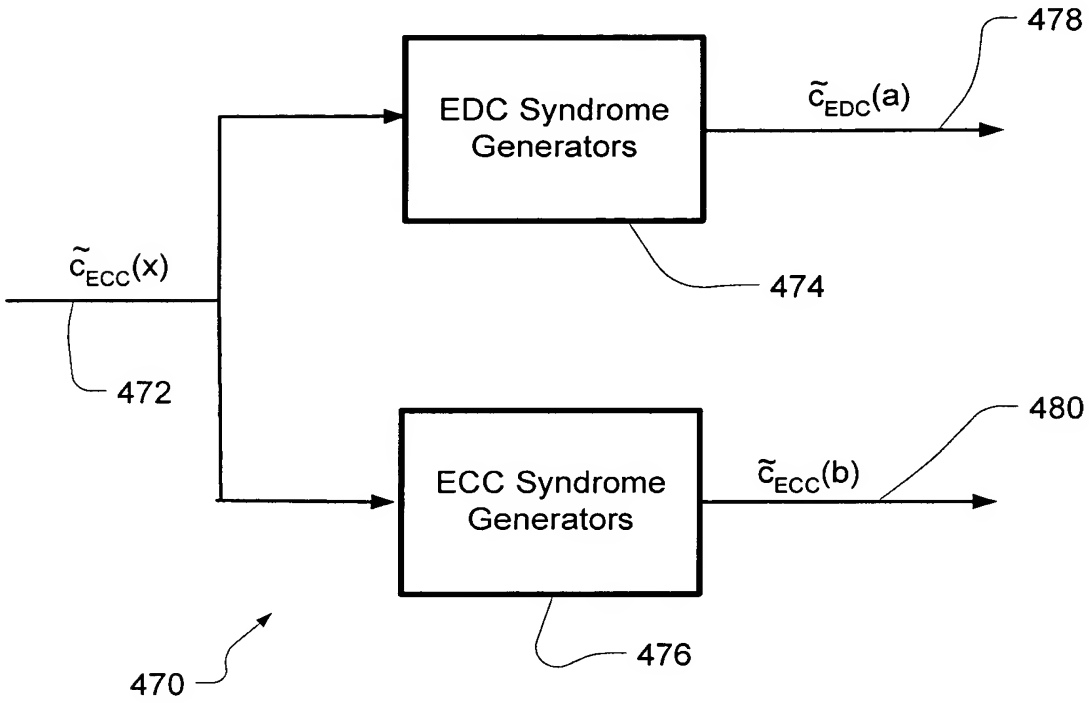

478
EDC Syndrome Generators
$\tilde{c}_{EDC}(a)$
$\tilde{c}_{ECC}(x)$
474
472
480
ECC Syndrome Generators
$\tilde{c}_{ECC}(b)$
476
470

FIG. 16

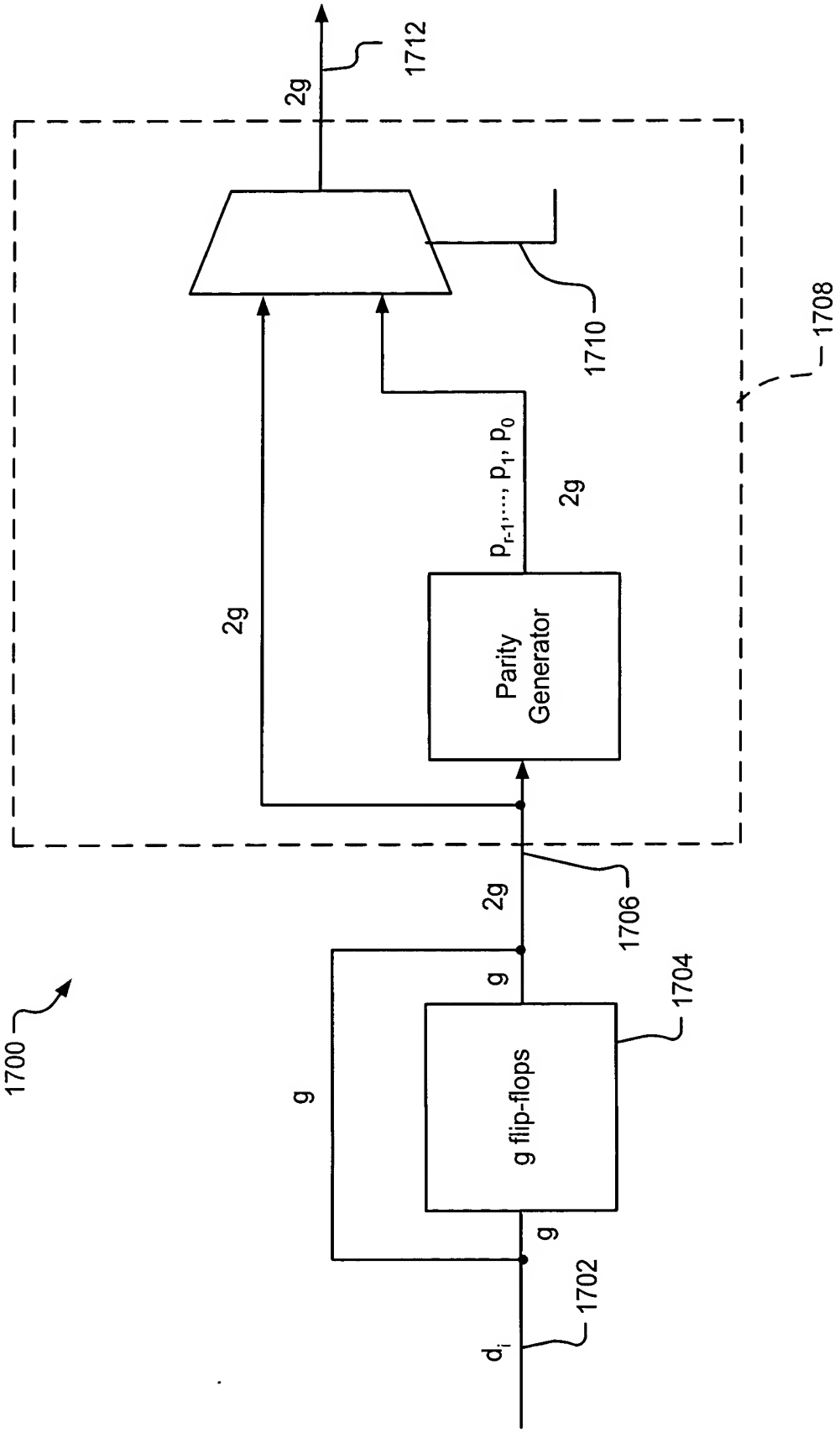

1700
1702
1704
1706
1708
1710
1712
g flip-flops
Parity Generator
g
2g
d_i
$p_{r-1}, \ldots, p_1, p_0$

FIG. 17

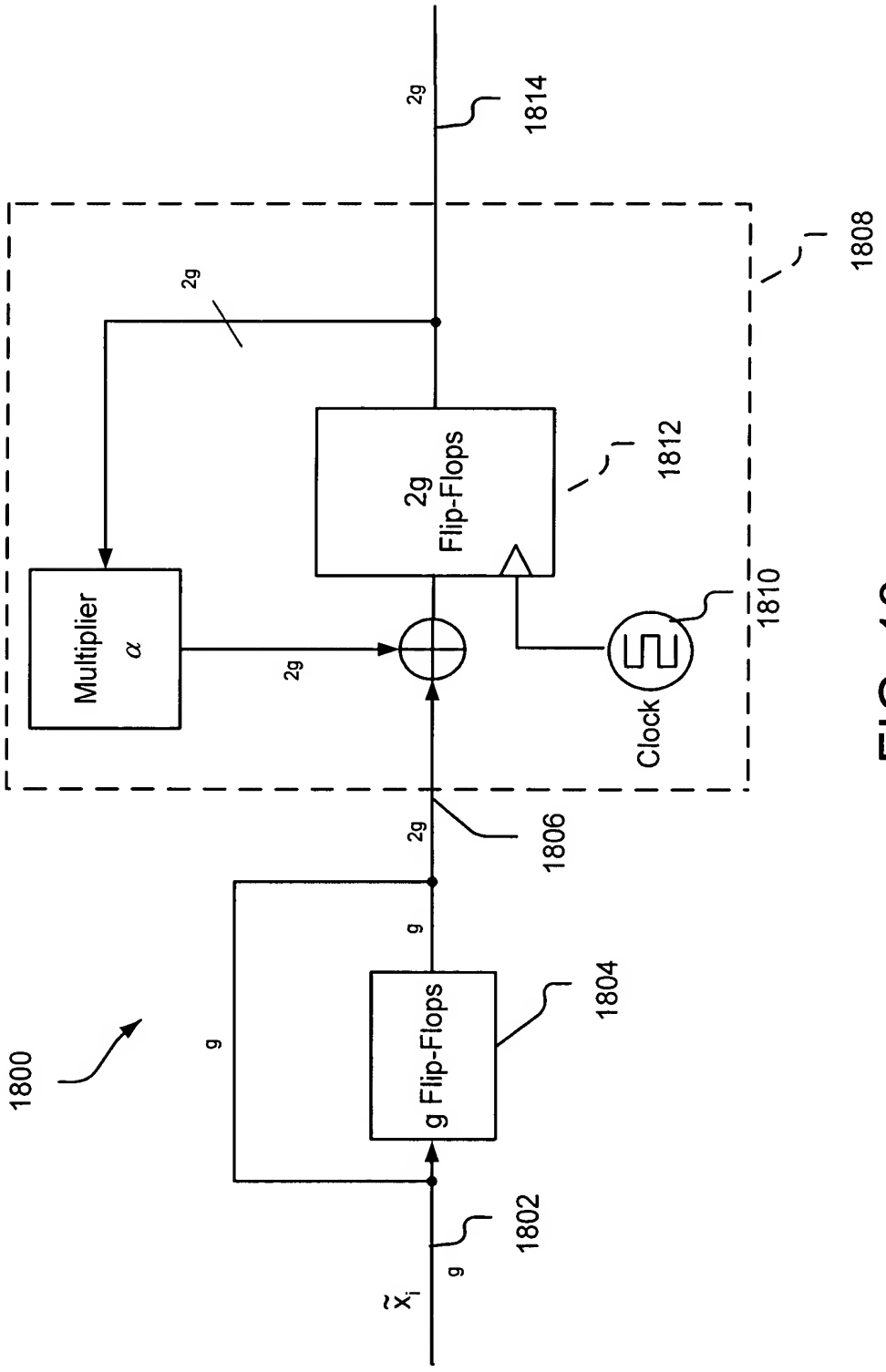

1800
1802
1804
1806
1808
1810
1812
1814
g Flip-Flops
2g Flip-Flops
Multiplier α
Clock
2g
g

FIG. 18

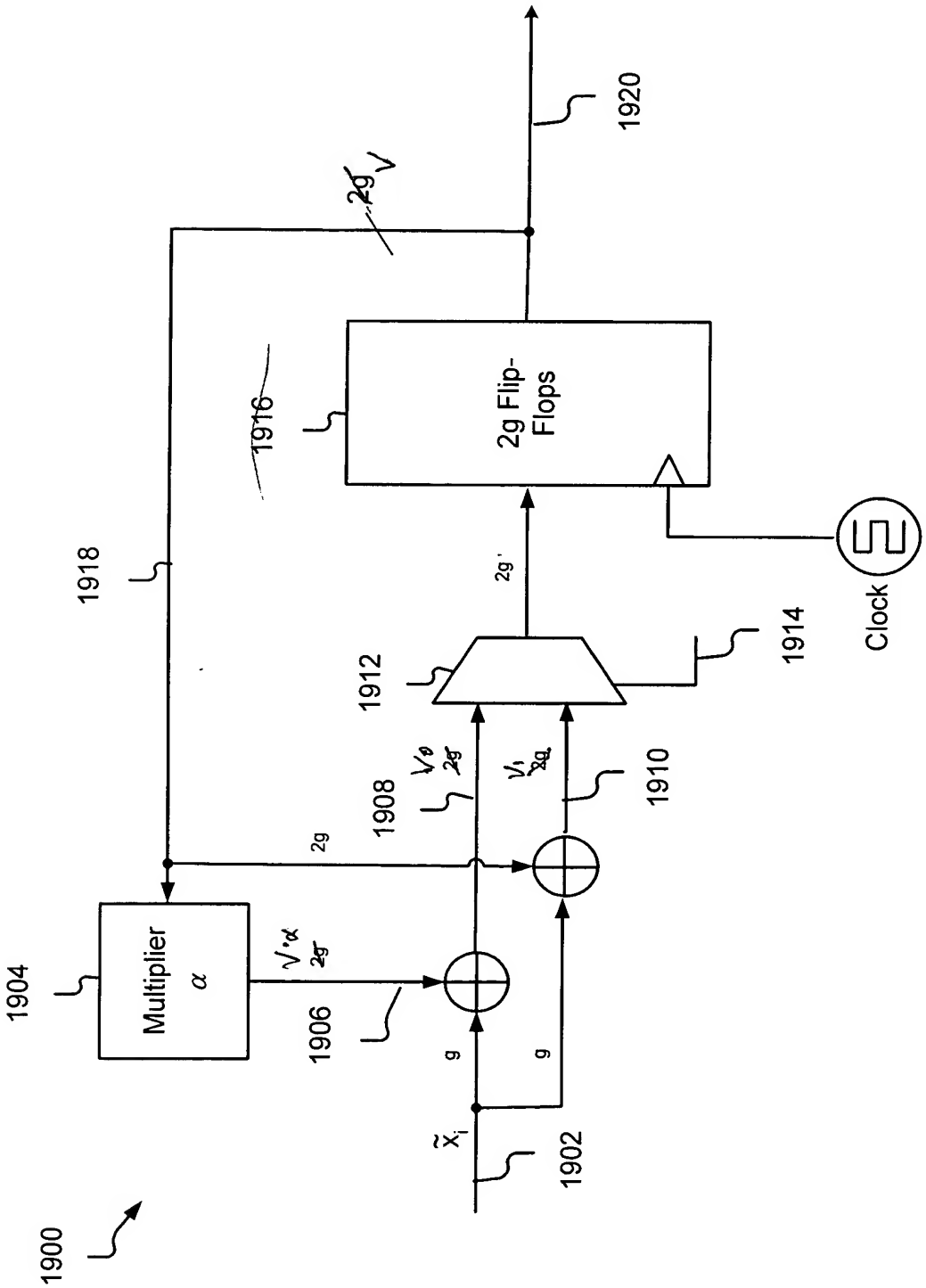

1900
1902
1904
Multiplier
α
1906
1908
1910
1912
1914
Clock
1916
2g Flip-
Flops
1918
1920
2g
2g '
g
g

FIG. 19

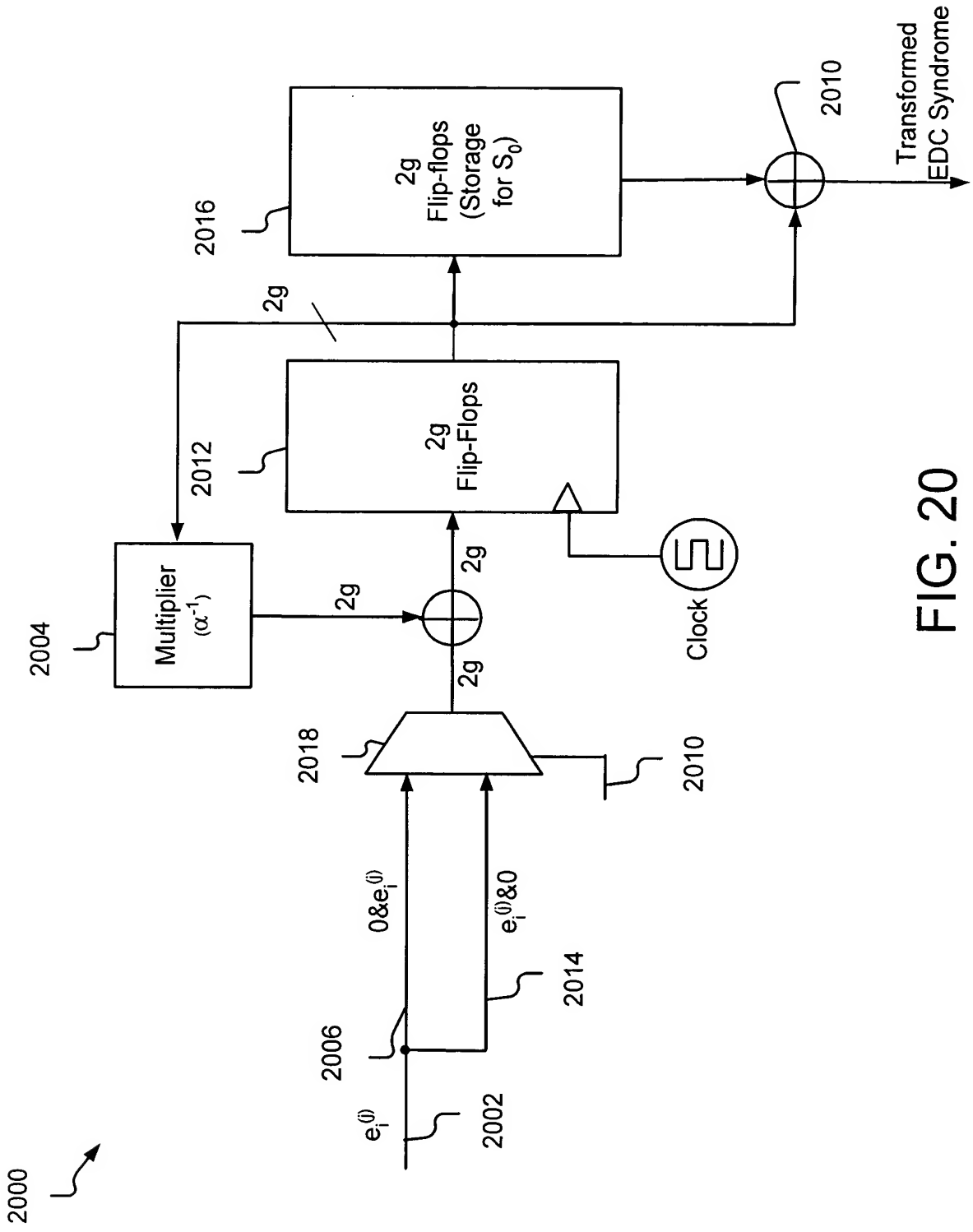

2000
2002
$e_i^{(i)}$
2006
$0\&e_i^{(i)}$
$e_i^{(i)}\&0$
2014
2018
2010
2004
Multiplier
(α^{-1})
2g
2012
2g
Flip-Flops
Clock
2016
2g
Flip-flops
(Storage
for S_0)
2010
Transformed
EDC Syndrome

FIG. 20

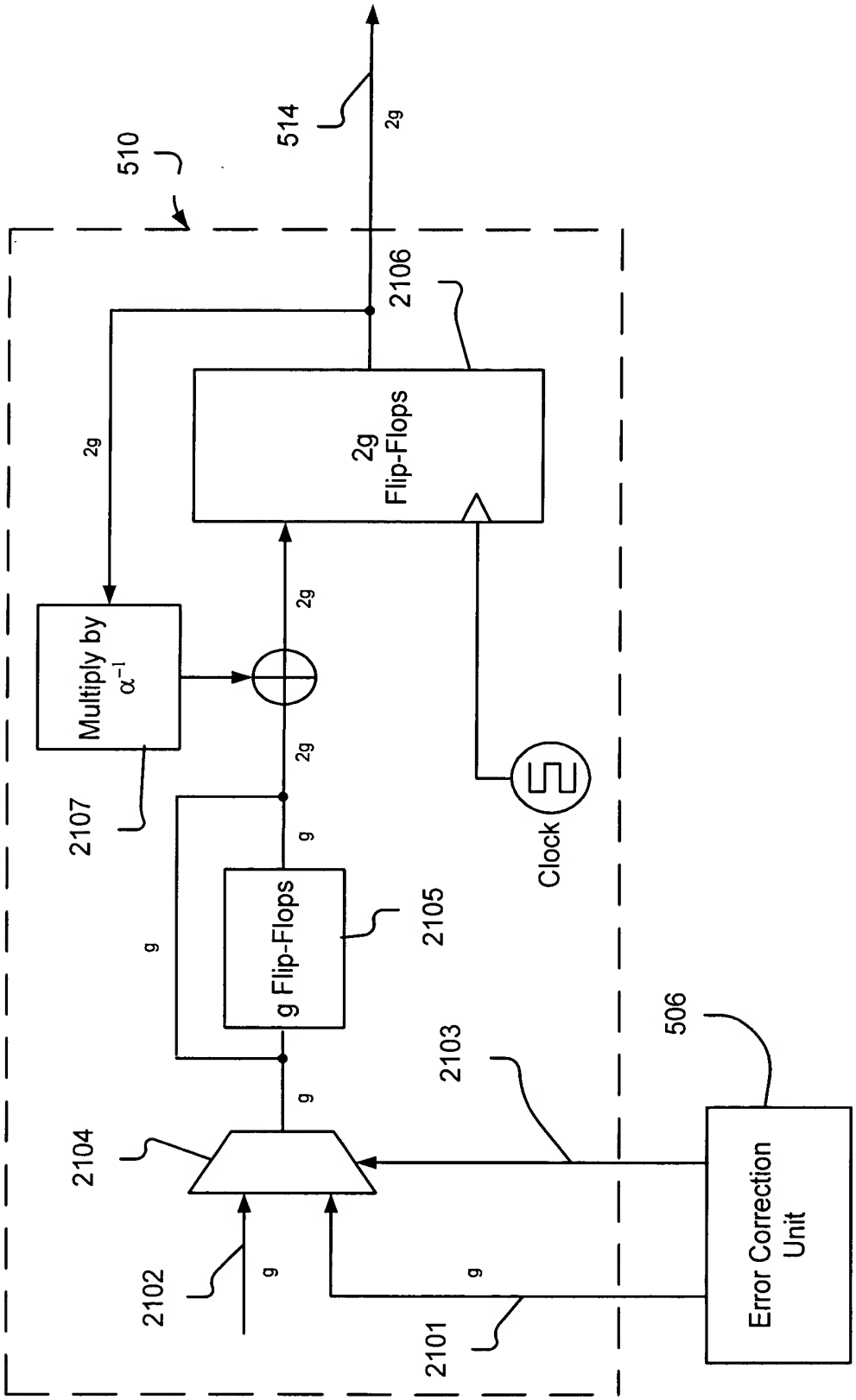

510
514
2g
2106
2g Flip-Flops
2g
Multiply by α^{-1}
2g
2107
g
g Flip-Flops
2105
Clock
g
2104
2103
506
Error Correction Unit
2102
g
g
2101

FIG. 21